In the Specification:

Please amend paragraph 0005, beginning on page 2 as follows:

In one embodiment of the invention, a trench in a surface of a single crystal silicon body, such trench having vertical sidewalls disposed in different crystallographic planes, one of such planes being the <100> crystallographic plane and another one of such planes being the <110> plane. A substantially uniform layer of silicon nitride is formed on the sidewalls of the trench. [[T he]] The trench, with the with substantially uniform layer of silicon nitride on the sidewalls thereof, is subjected to a silicon oxidation environment with sidewalls in the <110> plane being oxidized at a higher rate than sidewalls in the <100> plane producing silicon dioxide on the silicon nitride layer having thickness over the <110> plane greater than over the <100> plane. The silicon dioxide is subjected to an etch which selectively removes silicon dioxide while leaving substantially un-etched silicon nitride, such subjecting being for a time selected to remove portions of the silicon dioxide over the <100> plane to thereby expose underlying portions of the silicon nitride material while leaving portions of the silicon dioxide over the <110> plane on underlying portions of the silicon nitride material. Exposed portions of the silicon nitride material are selectively removed to expose underlying portions of the sidewalls of the trench disposed in the <100> plane while leaving substantially un-etched portions of the silicon nitride material disposed on sidewalls of the trench disposed in the <110> plane. The exposed underlying portions of the sidewalls of the trench disposed in the <100> plane and the un-etched portions of the silicon nitride material disposed on sidewalls of the trench disposed in the <110> plane are subjected to an silicon oxidation environment with the exposed sidewalls in the <100> plane being oxidized at substantially the same rate as the sidewalls in the <110> plane

having the un-etched silicon nitride material thereon to produce a substantially uniform silicon dioxide layer on the sidewalls of the trench.

Please amend paragraph 0011, beginning on page 3 as follows:

Referring now to FIG. 1A, a semiconductor structure 10, is shown. The structure 10 includes a single crystal silicon substrate 12 having formed in a upper surface 14 thereof a trench 16. Here, the substrate 12 is P type doped silicon. The upper surface 14 is here disposed in the <100> crystallographic plane of the silicon substrate 12. The trench 16 is a generally oval shape in the plane of the upper surface 14, as will be described in more detail in connection with FIG. 2A. Suffice it to say here, however, that because of the oval shape, shown dotted in FIG. 2A, it follows therefore that as shown in FIGs. 1A-1E, the vertical sidewalls 18 of the trench 16 are disposed in a number of different crystallographic planes, the most significant planes under consideration here are the <100> and <110> planes as shown in FIG. 2A by the hexagonal approximation to the oval shaped periphery of the trench 12.

Please amend paragraph 0013, beginning on page 4 as follows:

Referring now to FIG. 1B, the upper portions of the polycrystalline silicon conductor 30 are removed in any convention recessing process. Next, a trench top oxide (TTO) layer 34 is formed over the top portion of the trench 16, as indicated. The TTO 34 is a deposited oxide. The deposition of the TTO 34 results in a thinner deposition on the vertical sidewalls 18 of the trench 16 than on the polycrystalline silicon 30. Typically, the thickness of the TTO 34 on the sidewalls 18 is about 300 Angstroms and on the polycrystalline silicon 30 about 1000 Angstroms.

Please amend paragraph 0017, beginning on page 5 as follows:

Next, the structure shown in FIG. 2B, is placed in an oxidation environment to thermally grow a first silicon dioxide layer 42. It is noted that the thickness of the silicon dioxide layer 42 is dependent on the crystallographic plane in which the sidewall 18 of the silicon trench 16 is disposed. Here, however, the oxidation rate of the silicon is reduced on sidewalls 18 of the silicon substrate 12 having the silicon nitride layer 40. When the oxidation temperature is, for example, 750 to 1000 degrees Centigrade, the thickness of the silicon dioxide layer 42 on the vertical sidewalls 18 of the silicon trench in the <100> plane is half the thickness on the sidewalls of the silicon trench in the <110> plane. Further, if under such oxidation conditions, the silicon trench 16 sidewalls 18 were not covered with silicon nitride layer 40, growth of silicon dioxide layer to a thickness of 100 Angstroms on the sidewalls 18 in the <110> plane would yield a thickness of silicon dioxide layer of 50 Angstroms on the sidewalls in the <100> plane; however, if under the same oxidation conditions, the thin layer of silicon nitride were on the silicon sidewalls 18 of the trench, the thickness of the silicon dioxide over the sidewalls 18 in the <110> plane would be 50 Angstroms while the thickness of silicon dioxide over the sidewalls 18 in the <100> plane would be 25 Angstroms.

Please amend paragraph 0021, beginning on page 7 as follows:

Next, the structure shown in FIG. 2D is subjected to a second thermal oxidation process to form, at a relatively high oxidation rate on silicon sidewalls 18 in the <100> plane and at a lower (i.e., one-half) oxidation rate, on the silicon sidewalls in the <110> planes because of the presence of the silicon nitride on such sidewalls 18. The resulting structure is shown in FIG. 2E.

By choosing the proper nitridation, first and second oxidation thicknesses and oxidation process temperature, an optimum process can be designed for a target uniform silicon dioxide thickness ratio between the <100> and <110> plane thereby resulting in a substantially uniform gate oxide layer 44 on the vertical sidewall 18 if the silicon trench 16 independent of the crystallographic plane upon which the silicon dioxide layer 44 is grown. The resulting structure is shown in FIG. 1D and 2E; it being noted that there has been an out-diffusion of the dopant in the doped polycrystalline silicon 30 through a buried strap region 50 formed on the sidewalls 18 of the trench 16 between the bottom TTO 34 and the buried dielectric collar 28, as indicated. This diffusion region provides the source/drain region, here the drain region D, of the DRAM cell transistor and is electrically connected to the doped polycrystalline silicon 30 through the doped buried strap region 50.